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Title:

V_{cc} PUMP FOR CMOS IMAGERS

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Vcc PUMP FOR CMOS IMAGERS

Field of the Invention

5 The invention relates generally to improved semiconductor imaging devices and in particular to an imaging device which can be fabricated using a standard CMOS process. Particularly, the invention relates to a CMOS imager
10 having an array of image sensing cells and to the driving signals which operate the cells.

Discussion of Related Art

15 There are a number of different types of semiconductor-based imagers, including charge coupled devices (CCDs), photodiode arrays, charge injection devices and hybrid focal plan arrays. CCDs are often employed for image
20 acquisition and enjoy a number of advantages which makes it the incumbent technology, particularly for small size imaging applications. CCDs are also capable of large formats with small pixel size and they employ low noise charge domain processing techniques. However, CCD imagers also suffer from a number of
25 disadvantages. For example, they are susceptible to radiation damage, they exhibit destructive read out over time, they require good light shielding to avoid image smear and they have a high power dissipation for large arrays. Additionally, while
30 offering high performance, CCD arrays are difficult to integrate with CMOS

processing in part due to a different processing technology and to their high capacitances, complicating the integration of on-chip drive and signal processing electronics with the CCD array. While there has been some attempts to integrate on-chip signal processing with the CCD array, these attempts have not been entirely successful. CCDs also must transfer an image by line charge transfers from pixel to pixel, requiring that the entire array be read out into a memory before individual pixels or groups of pixels can be accessed and processed. This takes time. CCDs may also suffer from incomplete charge transfer from pixel to pixel during charge transfer which also results in image smear.

Because of the inherent limitations in CCD technology, there is an interest in CMOS imagers for possible use as low cost imaging devices. A fully compatible CMOS sensor technology enabling a higher level of integration of an image array with associated processing circuits would be beneficial to many digital applications such as, for example, in cameras, scanners, machine vision systems, vehicle navigation systems, video telephones, computer input devices, surveillance systems, auto focus systems, star trackers, motion detection systems, image stabilization systems and data compression systems for high-definition television.

The advantages of CMOS imagers over CCD imagers are that CMOS imagers have a low voltage operation and low power consumption; CMOS imagers are compatible with integrated on-chip electronics (control logic and timing, image

processing, and signal conditioning such as A/D conversion); CMOS imagers allow random access to the image data; and CMOS imagers have lower fabrication costs as compared with the conventional CCD since standard CMOS processing techniques can be used. Additionally, low power consumption is achieved for CMOS imagers because only one row of pixels at a time needs to be active during the readout and there is no charge transfer (and associated switching) from pixel to pixel during image acquisition. On-chip integration of electronics is particularly advantageous because of the potential to perform many signal conditioning functions in the digital domain (versus analog signal processing) as well as to achieve a reduction in system size and cost.

A CMOS imager circuit includes a focal plane array of pixel cells, each one of the cells including either a photogate or a photodiode overlying a substrate for accumulating photo-generated charge in the underlying portion of the substrate. A readout circuit is connected to each pixel cell and includes at least an output field effect transistor formed in the substrate and a charge transfer section formed on the substrate adjacent the photogate or photodiode having a sensing node, typically a floating diffusion node, connected to the gate of an output transistor. The imager may include at least one electronic device such as a transistor for transferring charge from the underlying portion of the substrate to the floating diffusion node and one device, also typically a transistor, for resetting the node to a predetermined charge level prior to charge transference.

In a CMOS imager, the active elements of a pixel cell perform the necessary functions of: (1) photon to charge conversion; (2) accumulation of image charge; (3) transfer of charge to the floating diffusion node accompanied by charge amplification; (4) resetting the floating diffusion node to a known state before the transfer of charge to it; (5) selection of a pixel for readout; and (6) output and amplification of a signal representing pixel charge. Photo charge may be amplified when it moves from the initial charge accumulation region to the floating diffusion node. The charge at the floating diffusion node is typically converted to a pixel output voltage by a source follower output transistor. The photosensitive element of a CMOS imager pixel is typically either a depleted p-n junction photodiode or a field induced depletion region beneath a photogate. For photo diodes, image lag can be eliminated by completely depleting the photodiode upon readout.

CMOS imagers of the type discussed above are generally known as discussed, for example, in Nixon et al., "256 x 256 CMOS Active Pixel Sensor Camera-on-a-Chip," IEEE Journal of Solid-State Circuits, Vol. 31(12) pp. 2046-2050, 1996; Mendis et al, "CMOS Active Pixel Image Sensors," IEEE Transactions on Electron Devices, Vol. 41(3) pp. 452-453, 1994 as well as U.S. Patent No. 5,708,263 and U.S. Patent No. 5,471,515, which are herein incorporated by reference.

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To provide context for the invention, an exemplary CMOS imaging circuit is described below with reference to FIG. 1. The circuit described below, for example, includes a photogate for accumulating photo-generated charge in an underlying portion of the substrate. It should be understood that the CMOS imager may include a photodiode or other image to charge converting device, in lieu of a photogate, as the initial accumulator for photo-generated charge.

Reference is now made to FIG. 1 which shows a simplified circuit for a pixel of an exemplary CMOS imager using a photogate and having a pixel photodetector circuit 14 and a readout circuit 60. It should be understood that while FIG. 1 shows the circuitry for operation of a single pixel, that in practical use there will be an MxN array of pixels arranged in rows and columns with the pixels of the array accessed using row and column select circuitry, as described in more detail below.

The photodetector circuit 14 is shown in part as a cross-sectional view of a semiconductor substrate 16 typically a p-type silicon, having a surface well of p-type material 20. An optional layer 18 of p-type material may be used if desired, but is not required. Substrate 16 may be formed of, for example, Si, SiGe, Ge, and GaAs. Typically the entire substrate 16 is p-type doped silicon substrate and may contain a surface p-well 20 (with layer 18 omitted), but many other options are possible, such as, for example p on p- substrates, p on p+ substrates, p-wells in

n-type substrates or the like. The terms wafer or substrate used in the description includes any semiconductor-based structure having an exposed surface in which to form the circuit structure used in the invention. Wafer and substrate are to be understood as including , silicon-on-insulator (SOI) technology, silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure or foundation.

An insulating layer 22 such as, for example, silicon dioxide is formed on the upper surface of p-well 20. The p-type layer may be a p-well formed in substrate 16. A photogate 24 thin enough to pass radiant energy or of a material which passes radiant energy is formed on the insulating layer 22. The photogate 24 receives an applied control signal PG which causes the initial accumulation of pixel charges in n+ region 26. The n+ type region 26, adjacent one side of photogate 24, is formed in the upper surface of p-well 20. A transfer gate 28 is formed on insulating layer 22 between n+ type region 26 and a second n+ type region 30 formed in p-well 20. The n+ regions 26 and 30 and transfer gate 28 form a charge transfer transistor 29 which is controlled by a transfer signal TX. The n+ region 30 is typically called a floating diffusion region. It is also a node for

passing charge accumulated thereat to the gate of a source follower transistor 36 described below. A reset gate 32 is also formed on insulating layer 22 adjacent and between n+ type region 30 and another n+ region 34 which is also formed in p-well 20. The reset gate 32 and n+ regions 30 and 34 form a reset transistor 31 which is controlled by a reset signal RST. The n+ type region 34 is coupled to voltage source VDD, e.g., 5 volts. The transfer and reset transistors 29, 31 are n-channel transistors as described in this implementation of a CMOS imager circuit in a p-well. It should be understood that it is possible to implement a CMOS imager in an n-well in which case each of the transistors would be p-channel transistors. It should also be noted that while FIG. 1 shows the use of a transfer gate 28 and associated transistor 29, this structure provides advantages, but is not required.

Photodetector circuit 14 also includes two additional n-channel transistors, source follower transistor 36 and row select transistor 38. Transistors 36, 38 are coupled in series, source to drain, with the source of transistor 36 also coupled over lead 40 to voltage source VDD and the drain of transistor 38 coupled to a lead 42. The drain of row select transistor 38 is connected via conductor 42 to the drains of similar row select transistors for other pixels in a given pixel row. A load transistor 39 is also coupled between the drain of transistor 38 and a voltage source VSS, e.g. 0 volts. Transistor 39 is kept on by a signal VLN applied to its gate.

5 The imager includes a readout circuit 60 which includes a signal sample and hold (S/H) circuit including a S/H n-channel field effect transistor 62 and a signal storage capacitor 64 connected to the source follower transistor 36 through row transistor 38. The other side of the capacitor 64 is connected to a source voltage VSS. The upper side of the capacitor 64 is also connected to the gate of a p-channel output transistor 66. The drain of the output transistor 66 is connected through a column select transistor 68 to a signal sample output node VOUTS and through a load transistor 70 to the voltage supply VDD. A signal called "signal sample and hold" (SHS) briefly turns on the S/H transistor 62 after the charge accumulated beneath the photogate electrode 24 has been transferred to the floating diffusion node 30 and from there to the source follower transistor 36 and through row select transistor 38 to line 42, so that the capacitor 64 stores a voltage representing the amount of charge previously accumulated beneath the photogate electrode 24.

25 The readout circuit 60 also includes a reset sample and hold (S/H) circuit including a S/H transistor 72 and a signal storage capacitor 74 connected through the S/H transistor 72 and through the row select transistor 38 to the source of the source follower transistor 36. The other side of the capacitor 74 is connected to the source voltage VSS. The upper side of the capacitor 74 is also connected to the gate of a p-channel output transistor 76. The drain of the output transistor 76 is connected through a p-channel column select transistor 78 to a

reset sample output node VOUTR and through a load transistor 80 to the supply voltage VDD. A signal called "reset sample and hold" (SHR) briefly turns on the S/H transistor 72 immediately after the reset signal RST has caused reset transistor 31 to turn on and reset the potential of the floating diffusion node 30, so that the capacitor 74 stores the voltage to which the floating diffusion node 30 has been reset.

The readout circuit 60 provides correlated sampling of the potential of the floating diffusion node 30, first of the reset charge applied to node 30 by reset transistor 31 and then of the stored charge from the photogate 24. The two samplings of the diffusion node 30 charges produce respective output voltages VOUTR and VOUTS of the readout circuit 60. These voltages are then subtracted ($VOUTS - VOUTR$) by subtractor 82 to provide an output signal terminal 81 which is an image signal independent of pixel to pixel variations caused by fabrication variations in the reset voltage transistor 31 which might cause pixel to pixel variations in the output signal.

FIG. 2 illustrates a block diagram for a CMOS imager having a pixel array 200 with each pixel cell being constructed in the manner shown by element 14 of FIG. 1. FIG. 4 shows a 2x2 portion of pixel array 200. Pixel array 200 comprises a plurality of pixels arranged in a predetermined number of columns and rows. The pixels of each row in array 200 are all turned on at the same time by a

row select line, e.g., line 86, and the pixels of each column are selectively output by a column select line, e.g., line 42. A plurality of rows and column lines are provided for the entire array 200. The row lines are selectively activated by the row driver 210 in response to row address decoder 220 and the column select lines are selectively activated by the column driver 260 in response to column address decoder 270. Thus, a row and column address is provided for each pixel. The CMOS imager is operated by the control circuit 250 which controls address decoders 220, 270 for selecting the appropriate row and column lines for pixel readout, and row and column driver circuitry 210, 260 which apply driving voltage to the drive transistors of the selected row and column lines.

FIG. 3 shows a simplified timing diagram for the signals used to transfer charge out of photodetector circuit 14 of the FIG. 1 CMOS imager. The photogate signal PG is nominally set to 5V and the reset signal RST is nominally set at 2.5V. As can be seen from the figure, the process is begun at time t_0 by briefly pulsing reset voltage RST to 5V. The RST voltage, which is applied to the gate 32 of reset transistor 31, causes transistor 31 to turn on and the floating diffusion node 30 to charge to the VDD voltage present at n+ region 34 (less the voltage drop V_{th} of transistor 31). This resets the floating diffusion node 30 to a predetermined voltage ($V_{DD}-V_{th}$). The charge on floating diffusion node 30 is applied to the gate of the source follower transistor 36 to control the current passing through transistor 38, which has been turned on by a row select (ROW)

signal, and load transistor 39. This current is translated into a voltage on line 42
 which is next sampled by providing a SHR signal to the S/H transistor 72 which
 charges capacitor 74 with the source follower transistor output voltage on line 42
 representing the reset charge present at floating diffusion node 30. The PG signal
 is next pulsed to 0 volts, causing charge to be collected in n+ region 26. A transfer
 gate voltage TX, similar to the reset pulse RST, is then applied to transfer gate 28
 of transistor 29 to cause the charge in n+ region 26 to transfer to floating diffusion
 node 30. It should be understood that for the case of a photogate, the transfer
 gate voltage TX may be pulsed or held to a fixed DC potential. For the
 implementation of a photodiode with a transfer gate, the transfer gate voltage TX
 must be pulsed. The new output voltage on line 42 generated by source follower
 transistor 36 current is then sampled onto capacitor 64 by enabling the sample and
 hold switch 62 by signal SHS. The column select signal is next applied to
 transistors 68 and 70 and the respective charges stored in capacitors 64 and 74 are
 subtracted in subtractor 82 to provide a pixel output signal at terminal 81.

It should also be noted that CMOS imagers may dispense with the
 transfer gate 28 and associated transistor 29, or retain these structures while biasing
 the transfer transistor 29 to an always "on" state.

The operation of the charge collection of the CMOS imager is known in
 the art and is described in several publications such as Mendis et al., "Progress in

CMOS Active Pixel Image Sensors," SPIE Vol. 2172, pp. 19-29 1994; Mendis et al., "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems," IEEE Journal of Solid State Circuits, Vol. 32(2), 1997; and Eric R. Fossum, "CMOS Image Sensors: Electronic Camera on a Chip," IEDM Vol. 95 pages 17-25 (1995) as well as other publications. These references are incorporated herein by reference.

Prior CMOS imagers suffer from inconsistent noise effects, voltage drops and leakage across the reset transistor 31, the row select transistor 38 and the transfer transistor 29. These affect the dynamic range of the pixel output as well as the ability of the pixel to accurately depict an image. Moreover, due to imprecision in the fabrication process, the electrical properties of these transistors will vary from pixel to pixel causing inconsistent output for the same level of charge from pixel to pixel. Since the size of the pixel electrical signal is very small due to the collection of photons in the photo array, the signal to noise ratio of the pixel should be as high as possible and charge leakage within a pixel as low as possible. Moreover, pixel output and the leakage of charge must be as consistent as possible from pixel to pixel.

Summary of the Invention

The present invention is designed to improve variations in the reset
5 voltage and the leakage characteristics of a CMOS imager pixel while improving the
consistency of the pixel to pixel output of the pixel array and increasing the
dynamic range of the pixel output. This is accomplished by driving one or more of
10 the reset gate, transfer gate (if used) and the row select gate with one or more
charge pumps. The charge pump provides a higher voltage than the supply voltage
VDD to improve the gating operation of the reset, transfer and row select
transistors. The charge pump increases the voltage to the reset gate so that the
5 voltage drop across the reset transistor does not lower the VDD reset charge at
floating diffusion node 30 and increases the voltage to the transfer gate to allow
barrier and well lowering in its operation. By overdriving one or more of the gates
of the reset, transfer and row select transistors with the output of a charge pump,
15 pixel to pixel fabrication differences in electrical characteristics of these transistors
can also be avoided. Moreover, if a photogate is used to acquire image charges this
too may be overdriven by an output voltage from a charge pump. Since the
25 photogate turn on voltage is typically VSS, e.g., 0 volts, a charge pump is used
which drives the photogate with an even lower voltage than VSS. Additionally, the
photogate may be overdriven, e.g. 6 volts, during charge collection to assure that
30 charge is effectively collected by the device.

The above and other advantages and features of the invention will be more clearly understood from the following detailed description which is provided in connection with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a representative circuit of the CMOS imager.

FIG. 2 is a block diagram of a CMOS active pixel sensor chip.

FIG. 3 is a representative timing diagram for the CMOS imager.

FIG. 4 is a representative pixel layout showing a 2x2 pixel layout according to one embodiment of the present invention.

FIG. 5 is a representative circuit drawing of a charge pump that may be used with the present invention.

FIG. 6 is an illustration of a computer system having a CMOS imager according to the present invention.

Detailed Description of the Preferred Embodiments

The present invention will now be described with reference to the figures. Reference is now made to FIG. 4. This figure shows a portion of an active pixel array constructed according to the present invention in which respective charge pumps 300, 301 and 302 are used to supply the gate voltages for the reset, transfer and row select transistors 31, 29 and 38. In addition, a charge pumps 303 and 304 are shown for providing a gate voltage to a photogate 24 for charge transfer and charge storage respectively. This figure shows a 2x2 array of pixels for simplification. It should be understood that the invention is directed to a MxN multiple pixel array of any size.

The operation of the FIG. 4 pixel array will now be described. Photodetectors 14 of a row of pixels are coupled via their respective row select transistors 38 to column line 42. The photodetector selected by a row decoder over line 86 will provide electrical current depending upon the voltage at the gate of source follower transistor 36 supplied by floating diffusion node 30. As noted, the gate of transistor 36 controls the current through load transistor 39 (not shown in FIG. 4) and in consequence the voltage on lead 42.

Signal ROW SELECT1 on lead 86 turns row select transistor 38 on. The voltage controlled by the row select signal 86 is a charge pump 302 output voltage. Row select 86 is connected to charge pump 302 to overdrive the row

select transistor, that is, the gate voltage of transistor 38 is higher than the VDD supply voltage. In a 5V VDD system, charge pump 302 will supply at least VDD+V_{th} volts to the gate of row select transistor 38 where V_{th} is the threshold voltage for transistor 38. The reset signal RST1 turns on transistor 31 which causes the floating diffusion node 30 to be reset to a potential of VDD-V_{th}, where V_{th} is the threshold voltage of the reset transistor 31. In the invention, the actual gate signal to transistor 31 is supplied by charge pump 300 to overdrive the gate of the reset transistor with a voltage of at least the value VDD+V_{th} to maintain a constant voltage reset value on node 30 at VDD. By having a higher reset voltage available at node 30, a wider dynamic response range is available for the pixel output signal and variation in the voltage at which the floating diffusion node 30 is reset due to the reset transistor 31 V_{th} variation is reduced.

The photogate 24 is also supplied from a charge pump 304, ensuring that the photogate to be overdriven to its on state to ensure that all possible collected charge for an image signal is stored in the imager substrate beneath the photogate until it is to be transferred out of the collection area. The photogate 24 is also supplied from a charge pump 303 in response to photogate signal PG over line 46, ensuring that the photogate to be overdriven to its on state to ensure that all possible collected charge for an image signal is transferred from the substrate beneath the photogate to the collection area.

The Fig. 4 circuit shows use of a transfer gate 28 and associated transistor 29. If the CMOS imager cells uses a transfer transistor, then the transfer gate 28 voltage is also supplied from a charge pump 301 in response to transfer signal TX, once again ensuring that the transfer transistor is overdriven to its on state and eliminating the V_{th} voltage drop which normally occurs. The operation of the FIG. 4 circuit to acquire, transfer and output pixel charge is otherwise as previously described.

In the invention, the charge pumps 300, 301 provide voltage to the reset gate 32 and transfer gate 28 at a potential which is greater than the supply potential VDD. The pumped voltage enhances the performance of the transfer and reset transistors. In order to turn "on" the various transistors of the pixel array, a gate voltage to the transistor must exceed a source or drain voltage (depending on the type of transistor) by a threshold voltage V_{th} . However, the threshold voltage (V_{th}) may differ for each transistor of a pixel array due to manufacturing imperfections. As a consequence, when all transistors of the array are turned "on" or "off" using the voltage supply potentials to supply control signals to the gates of the transistors, some transistors which are turned "on" are more "on" than other transistors thereby inconsistently transferring and/or amplifying the pixel charges transferred to the pixel output line 42. Likewise, some of the transistors which are turned "off" are more "off" than other transistors causing leakage. This is reflected

as an improper output of signals reflecting the charges collected by the photodetector circuit 14.

5 The charge pumps 300, 301, 302 and 304 help to overcome the inconsistent on/off threshold voltages (V_{th}) of the transistors by overdriving the gates with voltages which ensure that they turn on or off as required, regardless of manufacturing inconsistencies. Also, the charge pump 300 increases the dynamic
10 operating range of each pixel since the full reset voltage VDD will be applied to the floating diffusion node 30. The charge pump 303 ensures that the maximum possible charges are collected in the collection region beneath the photogate.

15 While multiple charge pumps 300, 301, 302, 303, 304 are shown in FIG. 4 for the entire CMOS pixel array, it should be understood that a single charge pump having multiple controlled output voltages may be used for the entire CMOS imager and for associated logic circuits. Also, individual charge pumps may
20 be used for different portions of the imager circuit and for the associated logic. Also, while the charge pumps 300, 301, 302, 303, 304 are shown supplying
25 voltage for the reset gate, the transfer gate, the row select gate and the photogate, it should be understood that a charge pump may be used for one or more of these gates to achieve a benefit over conventional CMOS imagers which do not use a
30 charge pump.

Reference is now made to FIG. 5 which shows one exemplary charge pump which may be used for one or more of charge pumps 300, 301, 302, 303 and 304. Charge pumps, *per se*, are well known, such as those shown in U.S. Patent No. 5,038,325 which is herein incorporated by reference. The exemplary charge pump, shown in FIG. 5, uses two clamp circuits 320, 330. An oscillator 310 provides its output to first and second capacitors 315, 335. Clamp circuits 320, 330 are connected across the capacitors 315, 335. The oscillator 310 is a ring oscillator which can be adjusted to increase or decrease its output signal frequency.

An output transistor 325 is connected between node 350 of capacitors 315 and a circuit output 355 node. An input signal SIG, which might vary between VDD and VSS, is output as an elevated potential signal SIGp which may vary between VSS and VDDp where $VDDp > VDD$. Where the potential signal SIGp is desired to be less than the operating voltage, i.e., charge pump 303, the output signal SIGp which may vary between VSSp and VDD where $VSSp < VSS$.

Both clamp circuits 320, 330 turn on and off at the same time, but the connection of clamp circuit 330 across capacitor 335 and in series with the output transistor has the result that the operation of the second clamp circuit 330 causes the output transistor 325 to conduct when potential at the node 350 is at a high potential. The rising edge of the oscillator 310 couples a high voltage through the capacitors 315, 335 which shuts the clamps 320, 330 off and allows the nodes 350,

355 to go high. The falling edge of the output of the oscillator 310 couples a drop in potential through the capacitors 315, 335, at which point, the clamps 320, 330 turn on, preventing the nodes 350, 355 from going low. A decoupling capacitor 345 further cooperates with the charge pump 300 in order to provide a steady boosted output which is switched by input signal SIG.

For operating the photogate PG, the charge pump 303 is configured to supply an output voltage $VSSp$ where $VSSp < VSS$. For collecting charge in the photogate, the charge pump 304 is configured to supply an output voltage VPg where VPg is greater than input voltage VDD .

As noted, the particular construction of the charge pump is not critical to the invention and many circuits besides the FIG. 5 circuit can be used. A representative output voltages of charge pumps 300, 301, 302, 304 are 6.0, 6.0 and 6.0, respectively for a 5.0 volt VDD supply and assuming that the V_{th} of each of these transistors is less than 1.0 volts. The charge pump 303 output has a representative voltage value of -1 volt. It should be understood that the output of voltage charge pumps 300, 301, 302, 303 and 304 may vary, individually, depending upon the VDD and/or VSS supply as well as the V_{th} of the individual transistors.

A typical processor based system which includes a CMOS imager device according to the present invention is illustrated generally at 400 in Fig. 6. A processor based system is exemplary of a system having digital circuits which could include CMOS imager devices. Such a system could include a computer system, camera system, scanner, machine vision system, vehicle navigation system, video phone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system and data compression system for high-definition television, all of which can utilize the present invention.

A processor system, such as a computer system, for example generally comprises a central processing unit (CPU) 444 that communicates with an input/output (I/O) device 446 over a bus 452. The CMOS imager 442 also communicates with the system over bus 452. The computer system 400 also includes random access memory (RAM) 448, and, in the case of a computer system may include peripheral devices such as a floppy disk drive 454 and a compact disk (CD) ROM drive 456 and I/O devices like a keyboard and/or mouse which also communicate with CPU 444 over the bus 452. CMOS imager 442 is preferably constructed as an integrated circuit which includes the voltage charge pumps 300, 301 and 302, as previously described with respect to FIGS. 4-7.

It should again be noted that although the invention has been described with specific reference to a CMOS imaging circuit having a photogate 24 and a

floating diffusion node 30, the invention has broader applicability and may be used in any CMOS imaging apparatus. Similarly, the process described above for charge collection, transfer and readout is but one method of many that could be used.

Accordingly, the above description and accompanying drawings are only illustrative of preferred embodiments which can achieve the features and advantages of the present invention. It is not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is only limited by the scope of the following claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is: